AMENDMENTS TO THE CLAIMS

1. **(Currently Amended)** A floating gate MOS transistor comprising:

one or more control gates;

an active channel;

at least one floating gate disposed substantially between ~~the control gate(s) and~~ the active channel and the one or more control gates;

first and second non-linear resistances coupling the floating gate to first and second control voltage sources respectively, the resistances forming a voltage divider network which sets the operating voltage of the floating gate.

2. **(Currently Amended)** A transistor according to claim 1, wherein said non-linear resistances are provided by respective diodes, ~~or transistors operating as diodes,~~ with the voltages applied to the first and second voltage sources being defined so that in use the diodes are reverse biased.

3. **(Previously Presented)** An electronic device comprising one or more floating gate transistors according to claim 1.

4. **(Original)** An electronic device according to claim 3, wherein the electronic device comprises means for varying the voltage applied to one or both of the first and second control voltage sources so that the operating voltage of the floating gate can be tuned to an appropriate value.

5. **(Previously Presented)** A method of operating the floating gate transistor of claim 1, the method comprising applying first and second fixed voltages to the first and second voltage sources respectively so as to set the floating gate to a desired operating voltage by an appropriate selection of the first and second voltages.

6. **(Previously Presented)** A method of operating the floating gate transistor of claim 1, the method comprising applying first and second voltages to the first and second voltage sources

respectively, at least one of the first and second voltages being variable so that the voltage at which the floating gate is operated can be set to a desired value by tuning one or both of the first and second voltages.

7. **(Currently Amended)** A floating gate MOS transistor comprising:

one or more control gates;

an active channel;

at least one floating gate disposed substantially between ~~the control gate(s) and~~ the active channel and the one or more control gates;

at least one non-linear resistance coupling the floating gate to a voltage source, the non-linear resistance being provided by a MOS transistor having its gate and source connected together, the transistor source being coupled to said voltage source and the transistor drain being coupled to the floating gate.

8. **(Original)** A transistor according to claim 7, the transistor gate being coupled to the transistor source via a resistance.

9. **(Currently Amended)** A floating gate MOS transistor comprising:

one or more control gates;

an active channel;

at least one floating gate disposed substantially between ~~the control gate(s) and~~ the active channel and the one or more control gates;

an insulating region surrounding the floating gate; and

a conductor at least partially surrounding said insulating region, wherein in use the conductor is coupled to an operating voltage.

10. **(Currently Amended)** A transistor according to claim 9, wherein a metal contact is formed on the floating gate, and a charge leakage path ~~extending~~ extends between the metal contact and said conductor.

11. **(Original)** A transistor according to claim 10, wherein the floating gate extends laterally from above the active channel, and said metal contact is formed on the floating gate at the end of the gate remote from the active channel.

12. **(Original)** A transistor according to claim 11, wherein said conductor surrounds an insulating region surrounding said metal contact and the adjacent portion of the floating gate.

13. **(Previously Presented)** An electronic device comprising one or more floating gate transistors according to claim 2.

14. **(Previously Presented)** A method of operating the floating gate transistor of claim 2, the method comprising applying first and second fixed voltages to the first and second voltage sources respectively so as to set the floating gate to a desired operating voltage by an appropriate selection of the first and second voltages.

15. **(Previously Presented)** A method of operating the floating gate transistor of claim 2, the method comprising applying first and second voltages to the first and second voltage sources respectively, at least one of the first and second voltages being variable so that the voltage at which the floating gate is operated can be set to a desired value by tuning one or both of the first and second voltages.

16. **(New)** A transistor according to claim 1, wherein said non-linear resistances comprise respective transistors operating as diodes, with the voltages applied to the first and second voltage sources being defined so that in use the diodes are reverse biased.

17. **(New)** An electronic device comprising one or more floating gate transistors according to claim 16.

18. **(New)** A method of operating the floating gate transistor of claim 16, the method comprising

applying first and second fixed voltages to the first and second voltage sources respectively so as to set the floating gate to a desired operating voltage by an appropriate selection of the first and second voltages.

19. **(New)** A method of operating the floating gate transistor of claim 16, the method comprising applying first and second voltages to the first and second voltage sources respectively, at least one of the first and second voltages being variable so that the voltage at which the floating gate is operated can be set to a desired value by tuning one or both of the first and second voltages.